WHAT IS CLAIMED IS:

1. An assembly for an LSI test which supplies a test signal output from an LSI tester to a target LSI to be tested and outputs, to the LSI tester, a test result signal generated by processing of the target LSI performed in accordance with the test signal,

the assembly comprising:

a peripheral circuit coupled to the target LSI and allowing the target LSI to operate in the same manner as in the application environment; and

a printed circuit board on which the peripheral circuit is mounted.

2. The assembly for an LSI test of claim 1, including:

a first board including the peripheral circuit and the printed circuit board; and

a second board coupled to the first board and including wiring for coupling the first board and the LSI tester to each other.

3. The assembly for an LSI test of claim 1, wherein the test signal is supplied to the peripheral circuit and then output from the peripheral circuit to the target LSI.

4. The assembly for an LSI test of claim 1, wherein the test result signal is supplied to the peripheral circuit and then output from the peripheral circuit to the LSI tester.

5. The assembly for an LSI test of claim 1, wherein a memory is provided as the peripheral circuit or in the target LSI, and

the LSI tester is configured to be capable of accessing the memory asynchronously to a clock supplied to the target LSI.

6. The assembly for an LSI test of claim 5, wherein the test signal is stored in the memory, and then read out from the memory to be processed by the target LSI.

7. The assembly for an LSI test of claim 5, wherein the test result signal is stored in the memory, and then read out from the memory to the LSI tester.

8. An assembly for an LSI test which supplies a test signal output from an LSI tester to a target LSI to be tested and outputs, to the LSI tester, a test result signal generated by processing of the target LSI performed in accordance with the test signal,

the assembly comprising:

a test result receiving circuit for performing given processing on data obtained as the test result signal so as to reduce the amount of the data, and for outputting a result of the processing to the LSI tester; and

a printed circuit board on which the test result receiving circuit is mounted.

9. The assembly for an LSI test of claim 8, wherein an enable control circuit for selecting necessary data from the data obtained as the test result signal and for outputting the selected data is provided in the test result receiving circuit or in the target LSI.

10. The assembly for an LSI test of claim 8, wherein the test result receiving circuit includes a compression circuit for compressing input data and outputting the compressed data.

11. The assembly for an LSI test of claim 8, wherein the test result receiving circuit includes a determination circuit for determining whether or not the input data

coincides with data to be input when the target LSI operates normally, and outputting a result of the determination.

12. An LSI test system, comprising:

an LSI tester for supplying a test signal to a target LSI to be tested; and

an assembly for an LSI test which outputs, to the LSI tester, a test result signal generated by processing of the target LSI performed in accordance with the test signal,

wherein the assembly comprises,

a peripheral circuit coupled to the target LSI and allowing the target LSI to operate in the same manner as in the application environment and

a printed circuit board on which the peripheral circuit is mounted.

13. An LSI test method, comprising the steps of:

operating a non-defective LSI, which is configured as a target LSI to be tested and has been confirmed to operate normally, in a circuit equivalent to a circuit actually used, and generating and storing a test signal and a reference test result signal, based on a signal supplied to the non-defective LSI and a signal output from the non-defective LSI, respectively; and

supplying the test signal to the target LSI to compare a test result signal generated by the target LSI in accordance with the test signal, with the reference test result signal, thereby determining whether or not the target LSI is defective.